WHAT IS CLAIMED IS:

1. A method for manufacturing a trench isolation on a silicon substrate, comprising:

forming a trench area for device isolation in the silicon substrate, wherein the trench has inner sidewalls;

forming an oxide layer on a surface of the silicon substrate that forms the inner sidewalls of the trench;

supplying healing elements to the silicon substrate to remove dangling bonds; and

filling the trench with a device isolation layer.

2. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 1, wherein the healing elements are fluorine.

3. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 1, wherein forming the oxide layer and supplying the healing elements are performed simultaneously through thermal annealing in a fluorine and oxygen gas atmosphere.

4. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 1, further comprising:

forming a silicon nitride layer as an oxygen barrier layer after supplying the healing elements to the silicon substrate and before filling the trench with the device isolation layer.

5. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 1, wherein supplying the healing elements is carried out by annealing the oxide layer in a gas atmosphere containing the healing elements, after forming the oxide layer on the surface of the substrate forming the inner sidewalls of the trench.

6. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 1, wherein supplying the healing elements comprises:

forming an ion implanting layer on the oxide layer;

implanting the healing elements in the ion implanting layer by an ion implantation; and

diffusing the ion implanted healing elements by means of a thermal annealing process.

7. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 6, wherein the ion implanting layer is a polysilicon layer.

8. A semiconductor device with a trench isolation, comprising:

a silicon substrate having a trench on a surface thereof;

a filling layer positioned in the trench for device isolation; and

a silicon oxide layer containing healing elements positioned between the filling layer and the silicon substrate.

9. The semiconductor device with a trench isolation as claimed in claim 8, wherein the healing elements are contained in an interface boundary between the silicon oxide layer and the substrate.

10. The semiconductor device with a trench isolation as claimed in claim 8, further comprising a silicon nitride layer as an oxide barrier layer between the silicon oxide layer and the filling layer.

11. The semiconductor device with a trench isolation as claimed in claim 8, wherein the filling layer comprises a spin-on-glass layer or a CVD layer.

12. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 1, wherein forming the trench comprises:

forming a trench etching mask; and

etching the silicon substrate using the trench etching mask to form the trench in the silicon substrate.

13. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 12, wherein forming the trench etching mask comprises:

forming a pad oxide layer on the silicon substrate;

forming an etching prevention or barrier layer on the pad oxide layer;

patterning the trench etching mask using a photolithography process;

etching through the pad oxide layer and the etching prevention or barrier layer; and

removing the photoresist pattern.

14. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 12, wherein the etching of the silicon substrate is accomplished by an anisotropic etch.

15. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 12, further comprising forming sloped sidewalls inside the trench while etching the silicon substrate.

16. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 13, wherein the etching prevention or barrier layer is a silicon nitride layer.

17. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 16, wherein the silicon nitride layer is deposited by CVD.

18. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 15, further comprising thermally oxidizing the sidewalls inside the trench to form a sidewall thermal oxide layer inside the trench.

19. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 18, wherein the thermal oxidation is conducted in a furnace or a rapid thermal process machine at approximately 700°C.

20. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 18, further comprising supplying fluorine gas or NF_3 containing fluorine during the thermal oxidation in order to allow the sidewall thermal oxide layer and the silicon substrate inside the trench to contain fluorine therein.

21. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 18, further comprising depositing a silicon nitride liner on the entire silicon substrate.

22. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 21, wherein the silicon nitride liner is deposited by CVD.

23. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 22, wherein the silicon nitride liner is deposited to a thickness of approximately 100 Angstroms.

24. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 22, further comprising forming a device isolation layer on the silicon nitride liner to fill the trench.

25. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 24, wherein the device isolation layer is a silicon oxide layer.

26. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 24, wherein the device isolation layer is deposited by CVD, (HDP) CVD or by a SOG process.

27. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 24, further comprising performing a chemical mechanical polishing to remove the device isolation layer outside of the trench area and expose the trench etching mask.

28. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 24, further comprising performing a wet etching process to etch the silicon nitride layer.

29. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 28, wherein the wet etching process is a phosphoric acid wet etching process.

30. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 24, further comprising removing the pad oxide layer to form a trench device isolation layer.

31. The method for manufacturing a trench isolation on a silicon substrate as claimed in claim 30, wherein the trench device isolation layer has about a same level of surface height as the silicon substrate